01-06-00

A

IN THE UNITED STATES
PATENT AND TRADEMARK OFFICE

Patent Application
Inventor(s): Patrik Larsson and Christopher J. Nicol
Case: Larsson 20-11
Title: System and Method For Filtering Echo/Next Signal Interference

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Enclosed please find the following papers relating to the above-identified application for patent:

1. Specification, Claims and Abstract;
2. three sheets of informal drawings;
3. an Assignment with Cover Sheet;
4. a Declaration and Power of Attorney; and
5. a stamped, self-addressed postcard

Claims As Filed				
	No. Filed	No. Extra	Rate	Calculations
Total Claims	22-20 =	2	x $22.00 =	$ 44.00
Independent Claims	3 - 3 =	0	x $82.00 =	$ 0.00
Multiple Dependent Claim(s), if applicable	0		x $270.00 =	$ 0.00
Basic Fee				$790.00
			Total Fee	$834.00

Please file the application and charge Lucent Technologies, Inc.'s Deposit Account No. 12-2325 the amount of $834.00 to cover the filing fee. Duplicate copies of this letter are enclosed. In the event of non-payment or improper payment of a required fee, the Commissioner is authorized to charge or credit Deposit Account No. 12-2325 as required to correct the error.

Please direct all correspondence to the undersigned at 226 St. Paul Street, Westfield, New Jersey 07090, and direct all telephone inquiries to the undersigned at (908) 654-8000. Please stamp and return the postcard to the

undersigned upon receipt in the Patent Office of the foregoing items.

Respectfully submitted,

Jean-Marc Zimmerman

Jean-Marc Zimmerman
Registration No. 36,978
Attorney for Applicant

Dated: January 5, 2000
JMZ/id
enclosures

Certificate of Express Mailing
Express Mail Label No. EJ163578138US
Date of Deposit: January 5, 2000

I hereby certify that the enclosed patent application for System and Method For Filtering Echo/Next Signal Interference is being sent Express Mail Post Office Service under 37 C.F.R. Section 1.10 on the date indicated above and are addressed to the Commissioner of Patents and Trademarks, Washington, D.C. 20231.

Jean-Marc Zimmerman

Jean-Marc Zimmerman

SYSTEM AND METHOD FOR FILTERING ECHO/NEXT SIGNAL INTERFERRENCE

FIELD OF THE INVENTION

The present invention pertains to the field of filters, and more particularly to finite impulse response (FIR) filters used for echo cancellation in communication systems.

BACKGROUND OF THE INVENTION

Conventional communications systems in which signals are transmitted through a cable have two principal types of signal interference. The first type of signal interference is an echo signal, in which a portion of a transmitted signal is reflected back toward the source of the signal. Such interference is caused by impedance mismatches associated with lumped elements of the system such as connectors and termination circuitry. The second type of signal interference is near end cross talk interference (NEXT) which is usually found in full-duplex bi-directional communications systems having a transmitter and a receiver coupled to a single wire of the cable and is generated across impedances in the cable and by the transmitter.

These echo/NEXT (E/N) interference signals are typically comprised of a few high energy echo signals and a large number of lower energy NEXT signals. Various

cancellation techniques are currently used to eliminate these types of interference. See "The Bell System Technical Journal," Vol. 59, No. 2, February 1980, pp. 149-159 and Data Communication Principles, R.R. Gitlin et al, pp 607-625.

When E/N cancellation (E/NC) methods are implemented in hardware as integrated FIR filters, a negative image for each one of the plurality of echo/Next (E/N) signals is digitally created from the transmitted signal, which is then summed with a received signal. FIR filters employ a plurality of taps in a delay line, wherein each tap is coincident with a particular interference signal. Unique multiplicand coefficients associated with each tap provide weighting to the time-sampled signals, and the plurality of weighted samples are summed to attain the desired filtered cancellation signal.

Conventional systems and methods for digitally filtering signals in the manner described above suffer from significant drawbacks. Specifically, such systems and methods employ a single FIR filter IC for filtering both low amplitude and high amplitude signals. However, filtering high bit resolution signals requires wide data paths which occupy large surface areas and consume large amounts of power thereby increasing the fabrication and operating costs of such devices. Moreover, since the bit resolution, chip

surface area, and power dissipation of all of the filters in a conventional FIR filter IC are identical and are designed to filter the highest amplitude E/N signal being filtered by the IC, using such devices to filter low amplitude signals is not cost effective or efficient from a performance standpoint.

SUMMARY OF THE INVENTION

We have developed in accordance with the principles of the invention a system and method for echo and near end cross talk (E/N) cancellation in a communications system using a pair of FIR filter ICs. The first FIR filter IC filters a plurality of low amplitude E/N signals and a first portion of a plurality of data bits of a plurality of high amplitude E/N signals, and the second FIR filter IC filters a second portion of data bits of the high amplitude E/N signals. The first portion of data bits of the high amplitude E/N signals comprises a certain number of least significant bits (LSBs) which are filtered by the first FIR filter IC, and the second portion of the high amplitude E/N signals comprises a certain number of most significant bits (MSBs) which cannot be filtered by the first FIR filter IC but are filtered by the second FIR filter IC. The output values from the two filters are then summed to produce the E/NC signal.

The bit resolution of the two FIR filter ICs is lower than the bit resolution which would be required to describe the largest signal in the E/N response. This allows for the use of lower bit-resolution, lower power consumption, and less expensive filter ICs than the conventional FIR filters implemented in a single IC.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 shows the energy reflection and leakage paths of a communications system of the present invention.

Figure 2 shows a plot of signal voltage amplitude in volts vs. tap number of the primary E/N signals shown in figure 1.

Figure 3 shows an exemplary embodiment of the FIR filter ICs of the present invention as they are implemented with the E/N signals shown in figures 1-2.

Figure 4 shows a tap arrangement used in each FIR filter shown in figure 3.

Figure 5 shows the bit partitioning performed by one of the taps shown in figure 4.

DETAILED DESCRIPTION OF THE DRAWINGS

The present invention is for a method and system for eliminating echo and near end crosstalk interference in conventional communications systems using FIR filters. Figure 1 shows the energy reflection and leakage paths of a communications system 10 according to the present invention, wherein a local circuit 12 includes a transmitter 14 and a receiver 16 which are both coupled to a switchable port 18 which is in turn coupled to transmission cable 20. System 10 also includes a remote circuit 22 coupled to cable 20 which is comprised of a remote receiver 24 and a remote transmitter 26 which are both coupled to a terminating port 28 with cable connectors. Depending on the application for which system 10 is used, one or more circuits 22 can be used, each one having different combinations of transmitter 26 and receiver 24.

Port 18 electrically isolates local receiver 16 from cable 20 while local transmitter 14 transmits data over cable 20. Port 18 also isolates local transmitter 14 from cable 20 while data is transmitted over cable 20 from remote transmitter 26. Transmitter 14 transmits data and receiver 16 receives data simultaneously over cable 20. An E/NC circuit 30 is included as part of circuit 12 and generates an E/N cancellation signal from a data signal transmitted by transmitter 14. This E/NC signal negates any corresponding E/N interference signal generated by transmission of the

data signal through port 18 and over transmission cable 20. Thus, a data signal at the input of receiver 16 includes none of the E/N interference signals. E/NC circuit 30 is comprised of two FIR filters ICs, which are each comprised of a plurality of FIR filters described below and shown in figures 3-5. Each one of the plurality of FIR filters is comprised of a plurality of filter elements.

Echo path 32 represents the internal E/N signal paths in circuit 12 from transmitter 14 to receiver 16 caused by parasitics associated with the interconnection of circuit boards of circuit 12 and the mirroring effects of the cable connectors at the port 18. Various other signal reflection and leakage paths are shown, i.e., crosstalk path 34 and echo path 36 which are generated by the near-end parasitics of cable 20, and crosstalk path 38 and echo path 40 which are generated by the far-end parasitics of cable 20 and the combination of the plurality of termination elements of circuit 22. Each of the E/N signals which are propagated along these paths are attenuated by the length of the paths traversed to receiver 16, with the more distant signals being more attenuated.

Figure 2 shows a plot of signal voltage amplitude in volts vs. Tap number of the primary E/N signals shown in Figure 1. The amplitude of the largest of these signals determines the bit resolution of the elements comprising the

FIR filters used in circuit 30. For example, if it assumed that E/N signal 42, which results from internal noise and reflection path 32 of circuit 12, is of sufficient amplitude to require 14 data bits to be accurately described within a given tolerance level, a FIR filter would have to provide 14 bit width data paths to accurately filter a sampled data word. Lower amplitude E/N signals require lower bit resolution. Typically, more than one E/N signal is associated with each lumped element, i.e., a plurality of wires, connectors, and/or ports.

Figure 2 also shows the relative voltage amplitudes of the plurality of near E/N signals shown in figure 1. E/N signal component 44 represents a signal that propagates along path 34 shown in figure 1, and E/N signal component 46 represents a signal that propagates along path 36 shown in figure 1. E/N signal components 42, 44 and 46 can be components of either a Next signal or an echo signal, with each component having a different source, e.g., a different connector. 44 and echo signal 46 are components of the same signal. The signal amplitudes shown in figure 2 are exemplary only, and may differ with various circuit topologies and different components that might vary E/N signal strength.

Figure 3 shows an exemplary embodiment of the FIR filter ICs of the present invention as they would be

implemented using the E/N signals shown in figures 1-2. A first FIR filter IC 48 is comprised of a plurality of lower bit-resolution FIR filters which process all of the data bits of a plurality of low amplitude signals and a portion of the data bits of a plurality of high amplitude signals, such as the three larger signals 42, 44 and 46 shown in figure 2. A second FIR filter IC 50 is comprised of three FIR filters 52, 54 and 56, which each process the portions of the data bits of high amplitude signals 42, 44 and 46, respectively, which are not processed by the first FIR filter IC.

If it is assumed the data path widths for the low resolution signals are eight bits wide, the 14 bit width data word of exemplary E/N signal 42 can be partitioned into an 8-bit and a 6-bit data word which are filtered by FIR filter ICs 48 and 50, respectively. The eight LSBs of E/N signal 42 can be processed by first FIR filter IC 48, and the remaining six MSBs can be processed by second FIR filter IC 50.

Adjustment of propagation delays of each tap signal coupled to FIR filters 52, 54 and 56 is occasionally necessary for proper operation of the cancellation circuitry 30 shown in Figure 1. This adjustment can be accomplished by using adaptively tunable delta-delays 58, wherein each tunable delay 58 is associated with one of FIR filters 52,

54 and 56. Alternatively, these adaptive delays can be implemented as register files, which are not shown, and are included in FIR filters 52, 54 and 56.

The configuration of the FIR filters comprising FIR filter ICs 48 and 50, respectively, need not be the same. Specifically, in FIR filter IC 50, FIR filter 52 can be in direct form while FIR filters 54 and 56 can be in transpose form. A gain stage 60 can be implemented as a simple shift register to achieve correct bit alignment between the filter elements of first FIR filter IC 48 and the filter elements of second FIR filter IC 50.

Figure 4 shows a tap arrangement used in FIR filters 52, 54 and 56 shown in Fig 3, wherein transmitted signal 62 is applied to a delay line 64, and time-delayed samples of signal 62 are obtained at taps 66, 68 and 70 residing on delay line 64. The operation of FIR filters, such as FIR filters 52, 54 and 56 shown in figure 3, are characterized by summing of a present signal sample with the weighted values of previous samples of the same signal. Since signal 62 propagates along delay line 64 over time, by providing taps at different locations along delay line 64, a plurality of samples of the delayed signal are available at any sampling instant. Each of these samples are multiplied by a unique weighting coefficient and then summed to produce the filtered value using the following transfer equation

$$C_m(f) = \sum_{-N}^{N} B_n e^{-j2\pi f\tau} \qquad (1)$$

where $C_m(f)$ is the filtered result of a given filter, $e^{-j2\pi f\tau}$ is the sinusoidal signal sampled at time τ, B_n is the weighting coefficient for the *n*th sample, and the number of delay samples at the filter taps is 2N+1 (-N to +N).

After signal 62 propagates along delay line 64, an instantaneous sampling of all the taps will produce a present time sample at tap 66, a previous time sample at tap 68, and a next previous time sample at tap 70. Each one of these samples is multiplied by the unique weighting coefficient associated with each particular tap. For example, the signal from tap 66 is multiplied in multiplier 72 by weighting coefficient B_n, the signal from tap 68 is multiplied in multiplier 74 by weighting coefficient B_{n-1}, and so on. The plurality of products of each tap chain are then summed in a mathematical adder 76 to produce a single filtered signal 78. Either fixed or floating point numbers can be used for the above operations.

Figure 5 shows the bit partitioning performed by one of the taps shown in figure 4. Specifically, a sampled data word of input signal 62 at tap 66 of delay line 64 is partitioned with the LSBs 80 of the sampled data word being processed by first FIR filter IC 48 and the MSBs 82 of the

sampled data word being processed by second FIR filter IC 50. If it is assumed that the eight LSBs of the 14 bit sampled data words associated with any one of the exemplary FIR filters 52, 54 and 56 shown in figure 3 are processed by first FIR filter IC 48, and the six MSBs of the sampled data words of FIR filters 52, 54 and 56 are processed by second FIR filter IC 50, first FIR filter IC 48 can be implemented as an 8-bit IC and second FIR filter IC 50 can be implemented as a 6-bit IC rather than all of the plurality of FIR filters of being implemented in a single expensive 14-bit IC. Alternatively, the partitioning can be implemented using any other combination of filter ICs, such as a 10-bit device and a 4-bit device, respectively. A final FIR output 84 is obtained by combining output 86 from FIR filter IC 48 and output 88 from FIR filter IC 50 at summing node 90.

Several methods can be used to partition a data signal using at least two FIR filter ICs according to the present invention. One method comprises the steps of determining from the plurality of E/N signals both a first bit resolution that describes at least a majority of the lowest amplitude E/N signals, and a second bit resolution that describes a single E/N signal having the highest amplitude. The first FIR filter IC is selected to have the first bit resolution and incorporates an LSB portion of all of the E/N

signals. The second FIR filter IC is selected to have a bit resolution that is equal to the difference between the second and first bit resolutions, such that the second FIR filter IC can filter any data bits of E/N signals that cannot be filtered by the first FIR filter IC.

A second method for partitioning data using the techniques described above is to halve the bit resolution that describes a single E/N signal having the highest amplitude to thereby obtain identical first and second bit resolutions. Thus, the data bits of higher amplitude signals can be evenly partitioned between the two FIR filter ICs, with the bits of the lower amplitude E/N signals being entirely filtered by the first FIR filter IC.

The number of lowest amplitude signals included in the aforementioned determination of the first bit resolution is controlled by the design criteria of the entire communications system, but should include at least half of all the signals to be filtered to insure that a representative first bit resolution is determined. Alternatively, inclusion of three-fourths of all the signals can be a requirement for the first bit resolution determination.

Partitioning data signals according to the present invention allows a plurality of smaller, less expensive filters to be used to filter Echo/NEXT interference signals

than a single conventional FIR filter used to filter such interference signals. This results in reductions in cost, IC chip size, and power dissipation compared to conventional filters.

The present invention can be used for applications other than data applications, such as voice applications.

Numerous modifications to the alternative embodiments of the present invention will be apparent to those skilled in the art in view of the foregoing description. Accordingly, this description is to be construed as illustrative only and is for the purpose of teaching those skilled in the art the best mode of carrying out the invention. Details of the structure may be varied substantially without departing from the spirit of the invention and the exclusive use of all modifications which come within the scope of the claims is reserved.

CLAIMS

What is claimed is:

1. An echo/near-end-crosstalk cancellation system for a bi-directional data communications system comprising:

a first finite impulse response (FIR) filter;

a second FIR filter coupled to the first FIR filter;

a data partitioning means for partitioning a data signal, wherein a first portion of the partitioned data signal is processed by the first FIR filter, and a second portion of the partitioned data signal is processed by the second FIR filter; and

a combination means for subtracting the outputs of the first and second FIR filters from the data signal to provide echo/near-end-crosstalk (E/N) cancellation.

2. The system according to Claim 1, further comprising a control means for adjusting the plurality of filter output values.

3. The system according to claim 1, wherein the first FIR filter and the second FIR filter are each implemented as a separate integrated circuit.

4. The system according to claim 1, wherein the first FIR filter is comprised of a plurality of filter elements.

5. The system according to claim 1, wherein the second FIR filter is comprised of a plurality of filter elements.

6. The system according to claim 1, wherein the data partitioning means comprises a plurality of conductors for conducting the first portion of the data signal to the first FIR filter and the second portion of the data signal to the second FIR filter.

7. The system according to claim 6, wherein the first portion of the partitioned data signal is comprised of the least significant bits (LSBs) of the data signal and the second portion is comprised of the most significant bits (MSBs) of the data signal.

8. The system according to claim 6, wherein the first portion of the partitioned data signal negates a first portion of an E/N signal generated as a result of the transmission of the data signal.

9. The system according to claim 8, wherein the second portion of the partitioned data signal negates a second portion of an E/N signal generated as a result of the transmission of the data signal, wherein the second portion of the E/N signal is not included in the first portion.

10. The system according to claim 1, wherein the first and second FIR filters are adaptive type filters.

11. The system according to claim 1, wherein the first and second FIR filters are non-adaptive type filters.

12. The system according to claim 1, wherein the first and second FIR filters are digital filters.

13. The system according to claim 1, wherein both the first and second FIR filters are configured identically in direct form.

14. The system according to claim 1, wherein both the first and second FIR filters are configured identically in transpose form.

15. The system according to claim 1, wherein the first and second FIR filters are configured differently, with one being in direct form and the other being in transpose form.

16. The system according to claim 1, wherein the control means for adjusting the plurality of filter output values comprises a multi-tap delay line including a plurality of taps, wherein at least one programmable delay line is interposed between two of the plurality of taps.

17. The system according to claim 1, wherein the control means for adjusting each of the plurality of filter output values comprises at least one holding register in each FIR filter for implementing a unique one of a plurality of adaptive delays.

18. The system according to claim 1, wherein the first and second FIR filters filter the data signal using either fixed or floating point numbers.

19. A method for partitioning data words in an echo/near-end-crosstalk cancellation circuit for a communications system, comprising the steps of:

determining a first bit resolution from a predetermined number of a plurality of echo/near-end-crosstalk (E/N) signals having a lowest amplitude;

determining a second bit resolution by subtracting the first bit resolution from a bit resolution of a single signal from a plurality of E/N signals having a highest amplitude; and

partitioning the plurality of E/N signals such that a first portion is processed by a first FIR filter having a data path identical to the first bit resolution, and a second portion comprised of bits having a data size exceeding the bit width of the first FIR filter is processed by a second FIR filter having a data path identical to the second bit resolution.

20. The method according to claim 19, wherein the predetermined number of signals comprises a majority of the plurality of E/N signals.

21. The method according to claim 20, wherein the predetermined number of signals comprises three quarters of the plurality of E/N signals.

22. A method for partitioning a data signal, comprising the steps of:

determining from a plurality of echo/near-end-crosstalk (E/N) signals a maximum bit resolution associated with a single signal having a highest amplitude;

selecting a first FIR filter and a second FIR filter each having a bit resolution equal to at least half of the maximum bit resolution; and

partitioning the plurality of E/N signals such that a first portion is processed by the first FIR filter, and a second portion comprised of bits having a data size greater than the bit width of the first FIR filter are processed by the second FIR filter.

ABSTRACT

A system and method for echo and near end cross talk (E/N) cancellation in a communications system using a pair of FIR filter ICs, wherein a first FIR filter IC filters a plurality of low amplitude E/N signals and a first portion of a plurality of data bits of a plurality of high amplitude E/N signals, and a second FIR filter IC filters a second portion of the data bits of the high amplitude E/N signals which cannot be filtered by the first FIR filter IC. The output values from the two filters are then summed to produce the E/N cancellation signal. The present invention allows for the use of lower bit-resolution, lower power consumption, and less expensive filter ICs than conventional FIR filters implemented in a single IC.

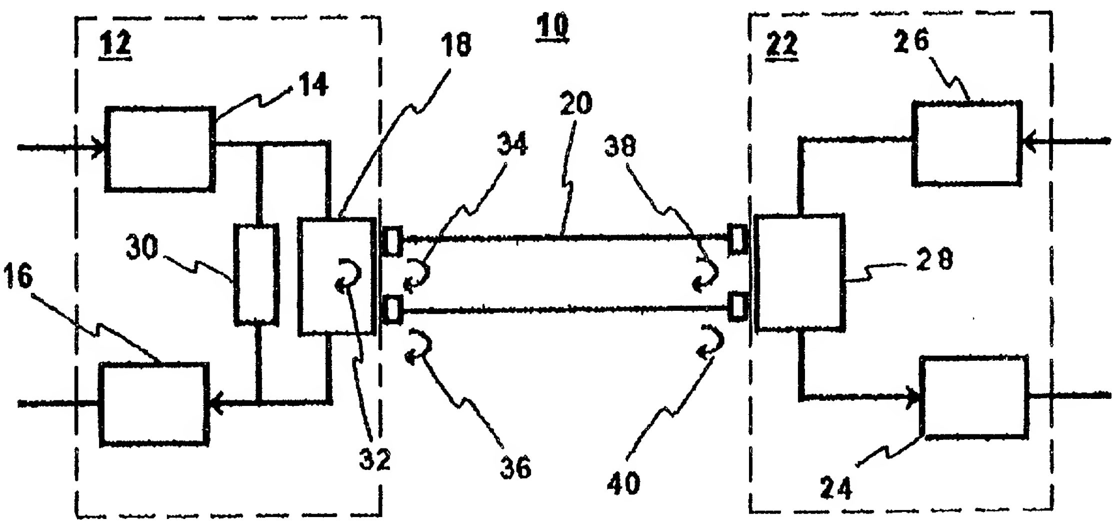


Fig. 1

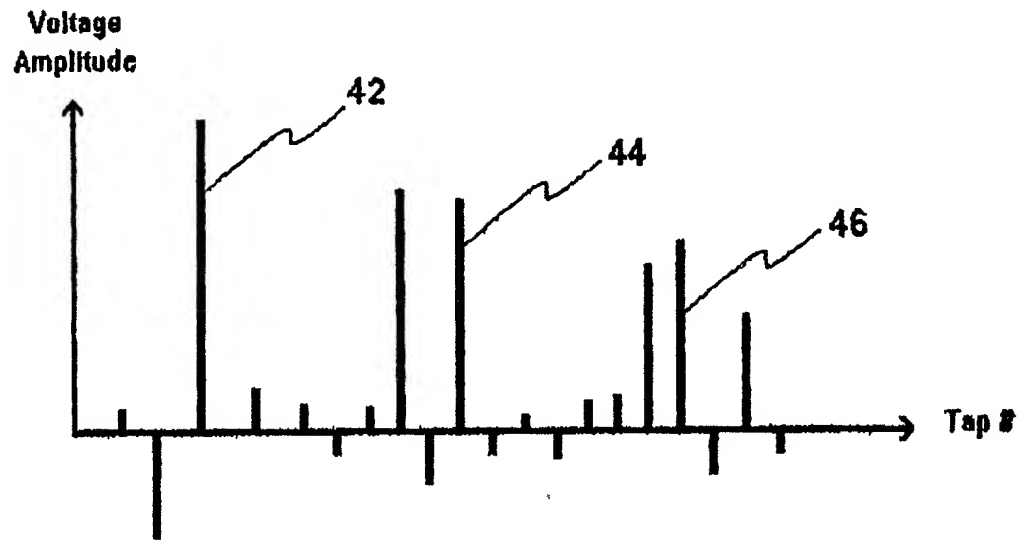


Fig. 2

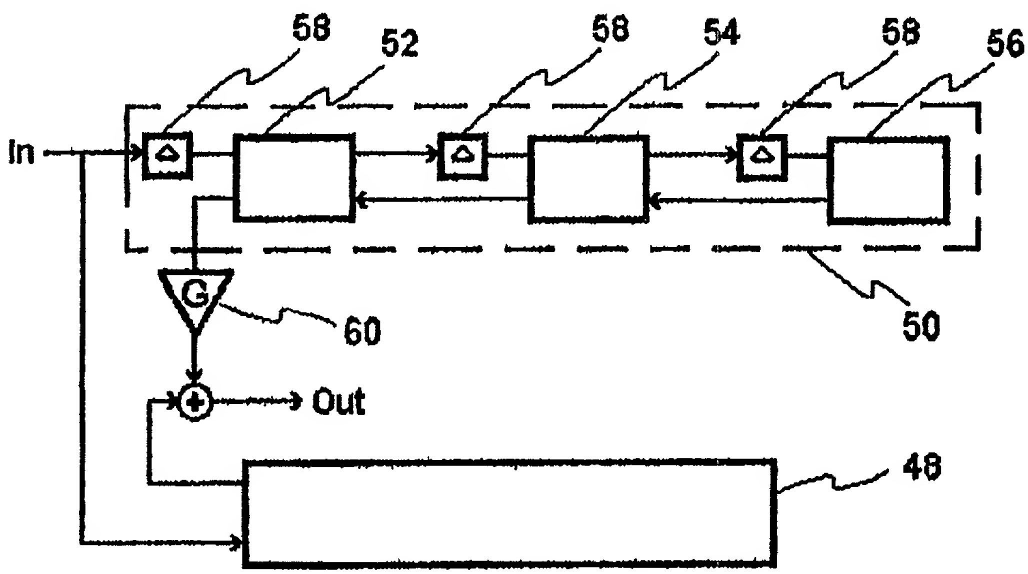
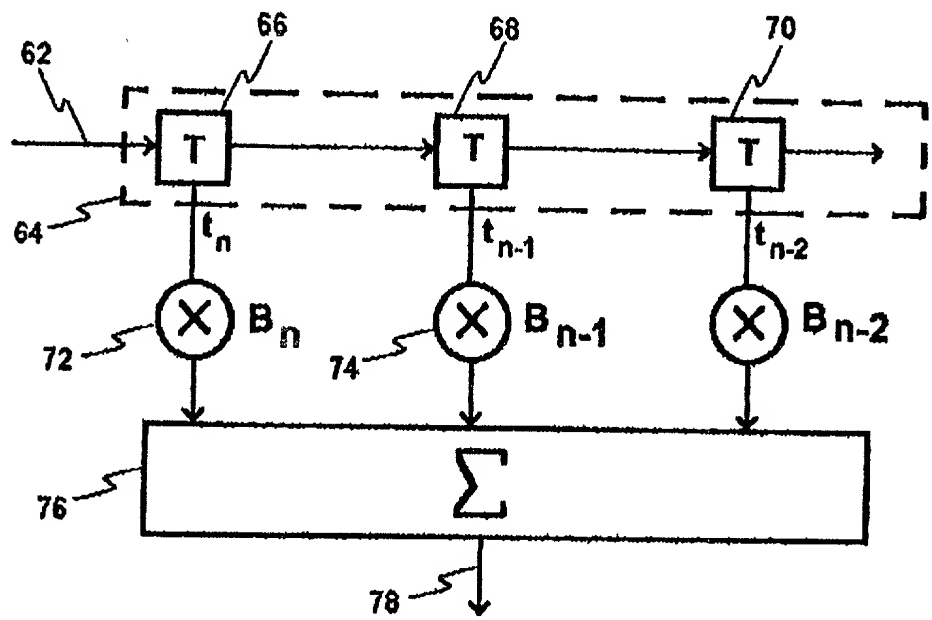
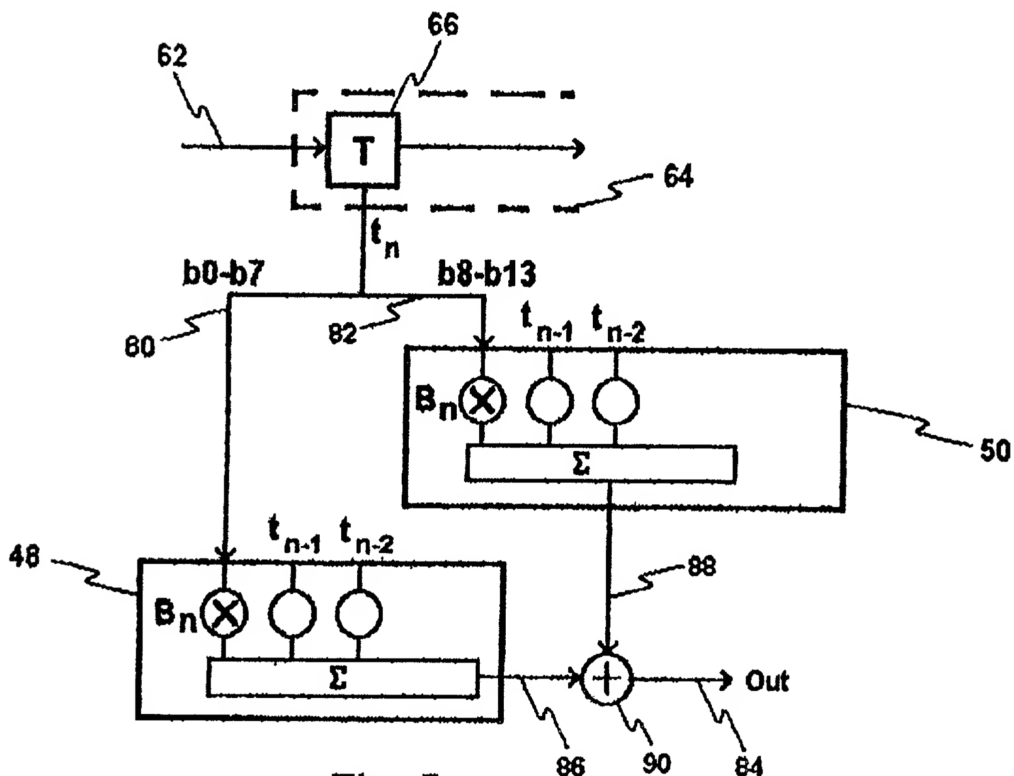


Fig. 3



62
66
68
70
64
T
T
T
t_n
t_{n-1}
t_{n-2}
72
74
B_n
B_{n-1}
B_{n-2}
76
Σ
78

Fig. 4



62
66
64
T
t_n
b0-b7
b8-b13
80
82
t_{n-1}
t_{n-2}
B_n
Σ
50
48
88
Σ
Out
86
90
84

Fig. 5

IN THE UNITED STATES
PATENT AND TRADEMARK OFFICE

Declaration and Power of Attorney

As the below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled System And Method For Filtering Echo/Next Signal Interferrence the specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by an amendment, if any, specifically referred to in this oath or declaration.

I acknowledge the duty to disclose all information known to me which is material to patentability as defined in Title 37, Code of Federal Regulations, 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

None

I hereby claim the benefit under Title 35, United States Code, 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

None

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

I hereby appoint the following attorney(s) with full power of substitution and revocation, to prosecute said application, to make alterations and amendments therein, to receive the patent, and to transact all business in the Patent and Trademark Office connected therewith:

Lester H. Birnbaum	(Reg. No. 25830)
Richard J. Botos	(Reg. No. 32016)
Jeffery J. Brosemer	(Reg. No. 36096)
Kenneth M. Brown	(Reg. No. 37590)
Donald P. Dinella	(Reg. No. 39961)
Guy Eriksen	(Reg. No. P-41736)
Martin I. Finston	(Reg. No. 31613)
James H. Fox	(Reg. No. 29379)
William S. Francos	(Reg. No. 38456)
Barry H Freedman	(Reg. No. 26166)
Julio A. Garceran	(Reg. No. 37138)
Mony R. Ghose	(Reg. No. 38159)
Jimmy Goo	(Reg. No. 36528)
Anthony Grillo	(Reg. No. 36535)
Stephen M. Gurey	(Reg. No. 27336)
John M. Harman	(Reg. No. 38173)
Donald E. Hayes, Jr.	(Reg. No. 33245)
John W. Hayes	(Reg. No. 33900)
Michael B. Johannesen	(Reg. No. 35557)
Mark A Kurisko	(Reg No. 38944)
Irena Lager	(Reg. No. 39260)
Christopher N. Malvone	(Reg. No. 34866)
Scott W. McLellan	(Reg. No. 30776)
Martin G. Meder	(Reg. No. 34674)
Geraldine Monteleone	(Reg. No. 40097)
John C. Moran	(Reg. No. 30782)
Michael A. Morra	(Reg. No. 28975)
Gregory J. Murgia	(Reg. No. 41209)
Claude R. Narcisse	(Reg. No. 38979)
Joseph J. Opalach	(Reg. No 36229)
Neil R. Ormos	(Reg. No. 35309)
Eugen E. Pacher	(Reg. No. 29964)
Jack R. Penrod	(Reg. No. 31864)
Daniel J. Piotrowski	(Reg. No. P-42079)
Gregory C. Ranieri	(Reg. No. 29695)
Scott J. Rittman	(Reg. No. 39010)
Eugene J. Rosenthal	(Reg. No. 36658)
Bruce S. Schneider	(Reg. No. 27949)
Ronald D. Slusky	(Reg. No. 26585)
David L. Smith	(Reg. No. 30592)
Patricia A. Verlangieri	(Reg. No. P-42201)
John P. Veschi	(Reg. No. 39058)
David Volejnicek	(Reg. No. 29355)
Charles L. Warren	(Reg. No. 27407)
Eli Weiss	(Reg. No 17765)

I hereby appoint the attorney(s) on ATTACHMENT A as associate attorney(s) in the aforementioned application, with full power solely to prosecute said application, to make alterations and amendments therein, to receive the patent, and to transact all business in the Patent and Trademark Office connected with the prosecution of said application. No other powers are granted to such associate attorney(s) and such associate attorney(s) are specifically denied any power of substitution or revocation.

Full name of inventor: Patrik Larsson

Inventor's signature Patrik L Date Dec 29, 1999

Residence: Matawan, Monmouth County, New Jersey

Citizenship: Sweden

Post Office Address: 10A Stillwell Street
Matawan, New Jersey 07747

Full name of inventor: Christopher John Nicol

Inventor's signature________________________ Date__________

Residence: Springwood N.S.W, Australia

Citizenship: Australia

Post Office Address: 12 Chaseling Avenue
Springwood N.S.W. Australia

Larsson 20-11

ATTACHMENT A

Attorney Name(s): Jean-Marc Zimmerman Reg. No.: 36,978

Telephone calls should be made to Jean-Marc Zimmerman at:

Phone No.: (908) 654-8000

Fax No.: (908) 654-7207

All written communications are to be addressed to:

Jean-Marc Zimmerman
226 St. Paul Street
Westfield, NJ 07090